I CLAIM

1. A controller for controlling interfacing to a data link, the data link enabling data items relating to a number of data elements to be transferred in corresponding data slots of the data link, the controller comprising:

at least one channel, each channel comprising a data buffer for storing data items, and a control register associated with the data buffer and arranged to store control data, the control data being settable to define for which data element or data elements data items are to be stored in that data buffer; and

an interface mechanism for controlling the transfer of data items between the at least one channel and the data slots of the data link in dependence upon said control data.

2. A controller as claimed in Claim 1, wherein the data buffer of at least one of the at least one channels is arranged to store prior to transmission on the data link data items relating to one or more data elements as specified by the control data, and the interface mechanism is arranged to be responsive to the control data to transmit on the data link in the corresponding one or more data slots data items retrieved from the data buffer.

3. A controller as claimed in Claim 1, wherein the data buffer of at least one of the at least one channels is arranged to store data items received from the data link and relating to one or more data elements as specified by the control data, and the interface mechanism is arranged to be responsive to the control data to store in the data buffer data items received from the corresponding one or more data slots.

4. A controller as claimed in Claim 1, wherein each channel comprises a pair of said data buffers and their associated control registers, one of said data buffers being arranged to store data items to be transmitted on the data link, and the other of said data buffers being arranged to store data items received from the data link.

5. A controller as claimed in Claim 1, wherein the number of channels provided by the controller is less than the number of data elements whose data items are capable of being transferred by the data link.

6. A controller as claimed in Claim 1, wherein each data buffer is arranged to store data items relating to one or more data elements having the same sampling rate.

7. A controller as claimed in Claim 1, wherein the controller is connectable to a codec via the data link.

8. A controller as claimed in Claim 1, wherein each data buffer comprises a first-in-first-out (FIFO) buffer.

9. A controller as claimed in Claim 1, further comprising a memory interface for coupling the controller to a memory, to enable data items to be transferred between the memory and the at least one channel.

10. A controller as claimed in Claim 9, wherein the memory interface couples the controller to the memory via a processor arranged to control access to the memory.

11. A controller as claimed in Claim 9, wherein each control register has a first field settable to indicate a compact mode in which data words passed between the associated data buffer and the memory comprise a plurality of said data items.

12. A controller as claimed in Claim 11, wherein data items are represented as a fixed size when transferred in the data slots, and each control register has a second field settable to indicate the actual size of data items stored in the associated data buffer, and if the first field is set the memory interface is arranged to reference the second field in order

to determine how many data items are to be included in each data word passed between the associated data buffer and the memory.

13. A controller as claimed in Claim 9, wherein data items are represented as a fixed size when transferred in the data slots, and each control register has a field settable to indicate the actual size of each data item stored in the associated data buffer, thereby enabling the memory interface to convert the data items between the actual size and the fixed size.

14. A controller as claimed in Claim 9, wherein the control data within the control register specifies the number of data elements whose data items are stored in the associated data buffer, and the memory interface is arranged to control the rate of transfer of data between the data buffer and the memory dependent on the control data.

15. A method of controlling interfacing to a data link, the data link enabling data items relating to a number of data elements to be transferred in corresponding data slots of the data link, the method comprising the steps of:

(a) providing at least one channel, each channel comprising a data buffer for storing data items, and a control register associated with the data buffer;

(b) storing control data in the control register to define for which data element or data elements data items are to be stored in the associated data buffer; and

(c) controlling the transfer of data items between the at least one channel and the data slots of the data link in dependence upon said control data.

16. A method as claimed in Claim 15, wherein the data buffer of at least one of the at least one channels is arranged to store prior to transmission on the data link data items relating to one or more data elements as specified by the control data, and the step (c) comprises being responsive to the control data to transmit on the data link in the corresponding one or more data slots data items retrieved from the data buffer.

17. A method as claimed in Claim 15, wherein the data buffer of at least one of the at least one channels is arranged to store data items received from the data link and relating to one or more data elements as specified by the control data, and the step (c) comprises being responsive to the control data to store in the data buffer data items received from the corresponding one or more data slots.